Amendments to the Claims:

This listing of the claims will replace all prior versions and listings of the claims in the application:

Listing of Claims:

1. (Canceled).

2. (Currently Amended) An integrated circuit ~~electrode~~ according to Claim 14 wherein the second metal also has higher oxygen affinity than the first metal.

3. (Canceled).

4. (Currently Amended) An integrated circuit ~~electrode~~ according to Claim 14 wherein the first metal is Ru and the second metal is Ta.

5. (Canceled).

6. (Canceled).

7. (Canceled).

8. (Canceled).

9. (Previously Presented) An integrated circuit comprising:

first spaced apart source and drain regions in an integrated circuit substrate;

a first gate insulating region on the integrated circuit substrate between the first spaced apart source and drain regions;

a first gate electrode on the first gate insulating region opposite the integrated circuit substrate, wherein the first gate electrode comprises an alloy comprising Ru and Ta;

second spaced apart source and drain regions in the integrated circuit substrate and of opposite conductivity type than the first spaced apart source and drain regions;

a second gate insulating region on the integrated circuit substrate between the second spaced apart source and drain regions; and

a second gate electrode on the second gate insulating region opposite the integrated circuit substrate, wherein the second gate electrode comprises an alloy comprising Ru and Ta and having different amounts of Ru relative to Ta than the first gate electrode.

10. (Previously Presented) An integrated circuit according to Claim 9 wherein the first spaced apart source and drain regions are n-type spaced apart source and drain regions and wherein the second spaced apart source and drain regions are p-type spaced apart source and drain regions.

11. (Previously Presented) An integrated circuit according to Claim 9 wherein the first spaced apart source and drain regions are n-type spaced apart source and drain regions, wherein the second spaced apart source and drain regions are p-type spaced apart source and drain regions and wherein the second gate electrode comprises a higher percentage of Ru relative to Ta than the first gate electrode.

12. (Previously Presented) An integrated circuit comprising:

n-type spaced apart source and drain regions in an integrated circuit substrate;

a first gate insulating region on the integrated circuit substrate between the n-type spaced apart source and drain regions;

a first gate electrode on the first gate insulating region opposite the integrated circuit substrate;

p-type spaced apart source and drain regions in the integrated circuit substrate;

a second gate insulating region on the integrated circuit substrate between the p-type spaced apart source and drain regions; and

a second gate electrode on the second gate insulating region opposite the integrated circuit substrate,

wherein the first gate electrode comprises an Ru-Ta alloy having between about 40% Ta and about 54% Ta and wherein the second gate electrode comprises an Ru-Ta alloy having less than about 20% Ta.

13. (Previously Presented) An integrated circuit comprising:

n-type spaced apart source and drain regions in an integrated circuit substrate;

a first gate insulating region on the integrated circuit substrate between the n-type spaced apart source and drain regions;

a first gate electrode on the first gate insulating region opposite the integrated circuit substrate;

p-type spaced apart source and drain regions in the integrated circuit substrate;

a second gate insulating region on the integrated circuit substrate between the p-type spaced apart source and drain regions; and

a second gate electrode on the second gate insulating region opposite the integrated circuit substrate,

wherein the first gate electrode comprises an Ru-Ta alloy having at least about 30% Ta and wherein the second gate electrode comprises an Ru-Ta alloy having less than about 30% Ta.

14. (Currently Amended) An integrated circuit comprising:

spaced apart source and drain regions in an integrated circuit substrate;

a first gate insulating region on the integrated circuit substrate between the spaced apart source and drain regions;

a first gate electrode on the first gate insulating region opposite the integrated circuit substrate, wherein the first gate electrode comprises an alloy comprising a first metal and a second metal having lower work function than the first metal;

a second gate insulating region on the integrated circuit substrate between the spaced apart source and drain regions; and

a second gate electrode on the second gate insulating region opposite the integrated circuit substrate, wherein the second gate electrode comprises an alloy

comprising [[a]] the first metal and [[a]] the second metal having lower work function than the first metal to provide a multiple gate integrated circuit field effect transistor.

15. (Currently Amended) An integrated circuit ~~electrode~~ according to Claim 14 wherein the first metal has a work function of greater than about 4.5eV and wherein the second metal has a work function of less than about 4.5eV.

16. (Currently Amended) An integrated circuit ~~electrode~~ according to Claim 14 wherein the first metal has a work function of about 5eV and wherein the second metal has a work function of about 4eV.

17. (Currently Amended) An integrated circuit ~~electrode~~ according to Claim 14 wherein the first metal has a work function of between about 5eV and about 5.2eV and wherein the second metal has a work function of between about 4eV and about 4.1eV.

18. (Currently Amended) An integrated circuit ~~electrode~~ according to Claim 14 wherein the first metal has a work function of between about 5eV and about 5.2eV and wherein the second metal has a work function of between about 3.5eV and about 4.0eV.

19-38. (Withdrawn)